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# Introduction

## Document SCOPE and Organization

## Acronyms

|  |  |
| --- | --- |
| **AD** | Applicable Document |
| **CGS** | Compagnia Generale per lo Spazio (formerly Carlo Gavazzi Space) |
| **NEOSTEL** | NEO Survey Telescope |
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## Applicable Documents

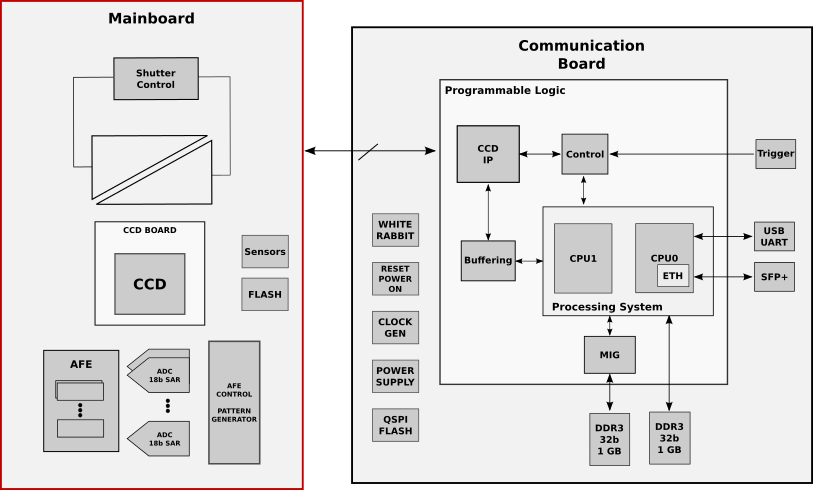
1. Statement of Work P2-NEO-V ‘NEO Survey Telescope Detailed Design’, SSA-NEO-TEL-SOW-0001, Issue 1, 17/12/2013
2. Space Situational Awareness - NEO System Requirements Document, SSA-NEO-RS-RD-0001, Issue 1, Revision 4, 05/04/2013
3. CGS Proposal “NEO Survey TELescope Design NEOSTEL”, S14-003 Is.1, April 2014

## Reference Documents

1. TELAD Design Report, TELAD-RP-CGS-001, version 1, 25/10/2011

# Hardware - Electronics

NEOSTEL camera hardware is designed to be modular. It consists of two main pieces: Communication Board and Mainboard with Analog Front-End. Principal parts and functions of the boards are presented on the block diagram below.

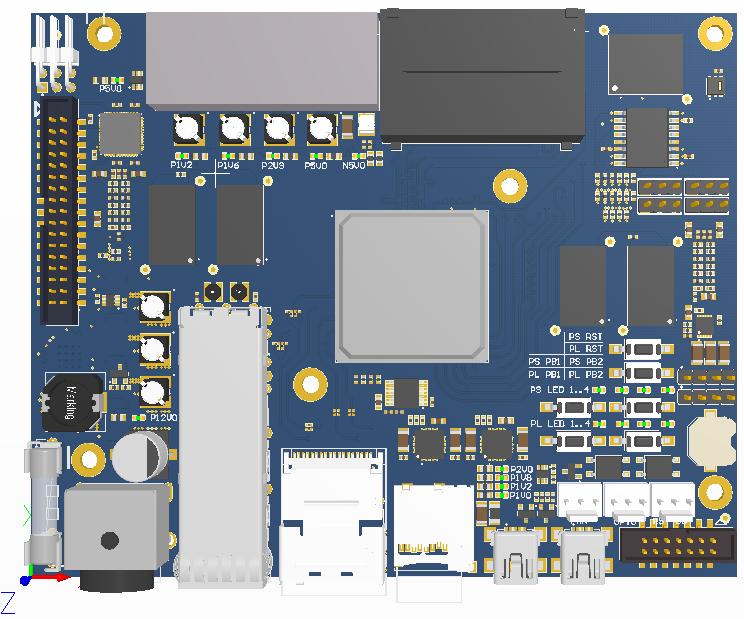


## Communication board

Communication board is placed on the Mainboard. It is intended to be an interface between CCD sensor and an external server. The role of this board is:

* generation of timing signals for CCD sensor
* generation of timing signals for Analog front-end module
* data collection from analog-to-digital converters
* communication over Ethernet
* time synchronization using PTP protocol

Main processing unit is Zynq SoC containing an ARM processor + FPGA architecture. This part supervisors all onboard peripherals and CCD sensor operations. It also sets proper voltage to supply and bias CCD, drives CCD signals, receives data from A/D converters and sends data over the Ethernet. Zynq has been chosen because of its ability to support 1 or 10 Gbit Ethernet. Zynq uses two types of the memory. The first is volatile (RAM), the second is non-volatile (FLASH). RAM memory keeps data and is required for image processing purposes, whereas FLASH contains the Linux file system. There is an additional storage device on the module - Micro SD card is used to store system logs. Ethernet connection is established by SFP/SFP+ transceiver. Thus copper or optical Ethernet connection can be implemented. Internal power supply consists of high efficiency DC/DC converter that supplies all of the devices on the module.



The picture above shows visualization of the Communication Board. It is designed to be 12-layers PCB of size of 125 mm x 100 mm.

## Mainboard

The Mainboard contains various subsystems designed to control and conduct acquisition processes. The board will also house connector to CCD Board and AFE module.

Analog Device's AD7960, 18bit SAR converters have been selected due to low noise, high SNR and relative high sampling rate. Four ADCs will be implemented to sample each channel – the goal is to oversample the signal and utilize digital signal processing to filter white and correlated noise. To lower the jitter of sampling clocks an additional buffer will be used.

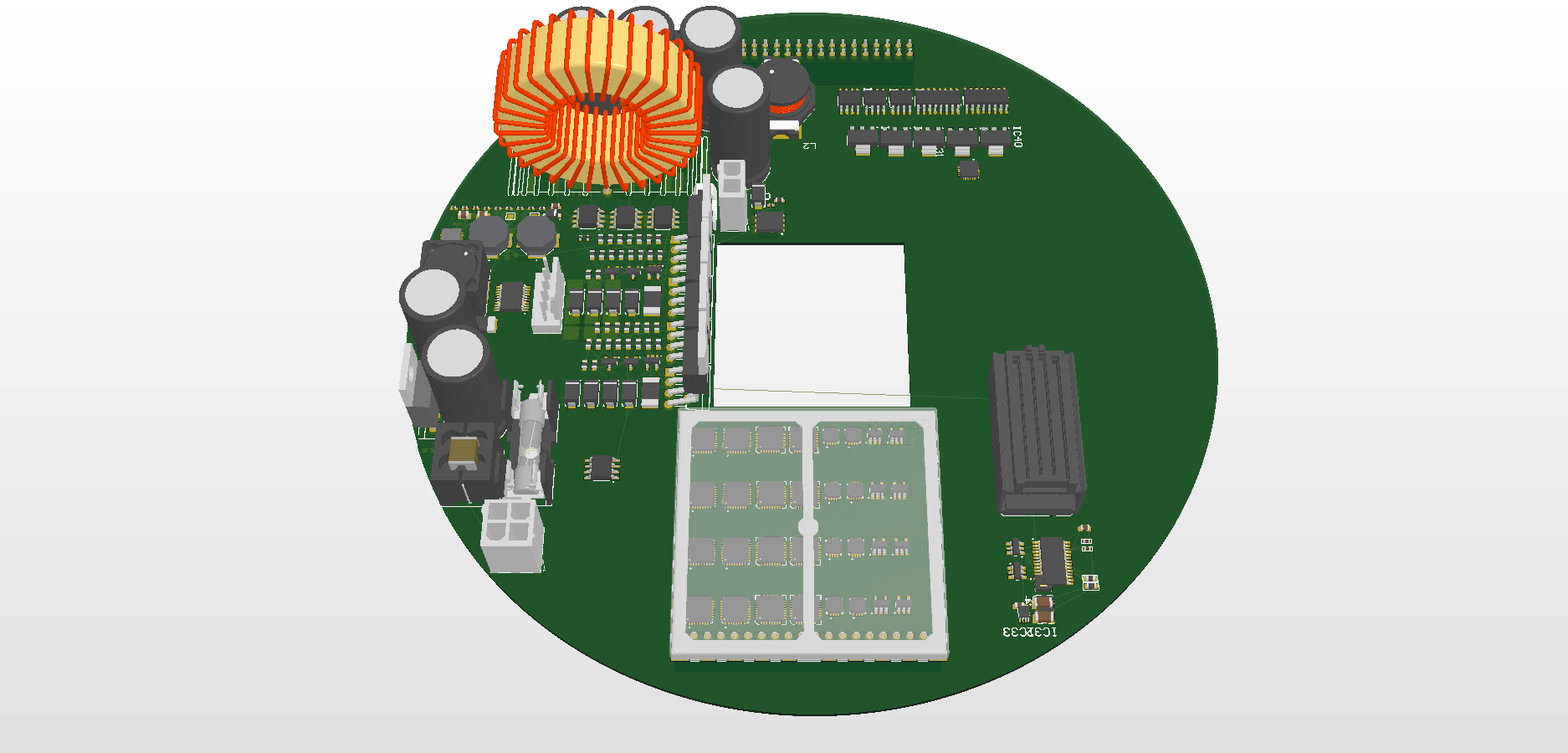
Analog-Front-End (AFE) board will contain circuitry designed to process raw analogue data from the CCD matrix. Depending on implementation it can be CDS, adaptive filtering and buffering of input signal. Several implementations are considered and the one with best noise characteristics will be used in the final version of the camera.

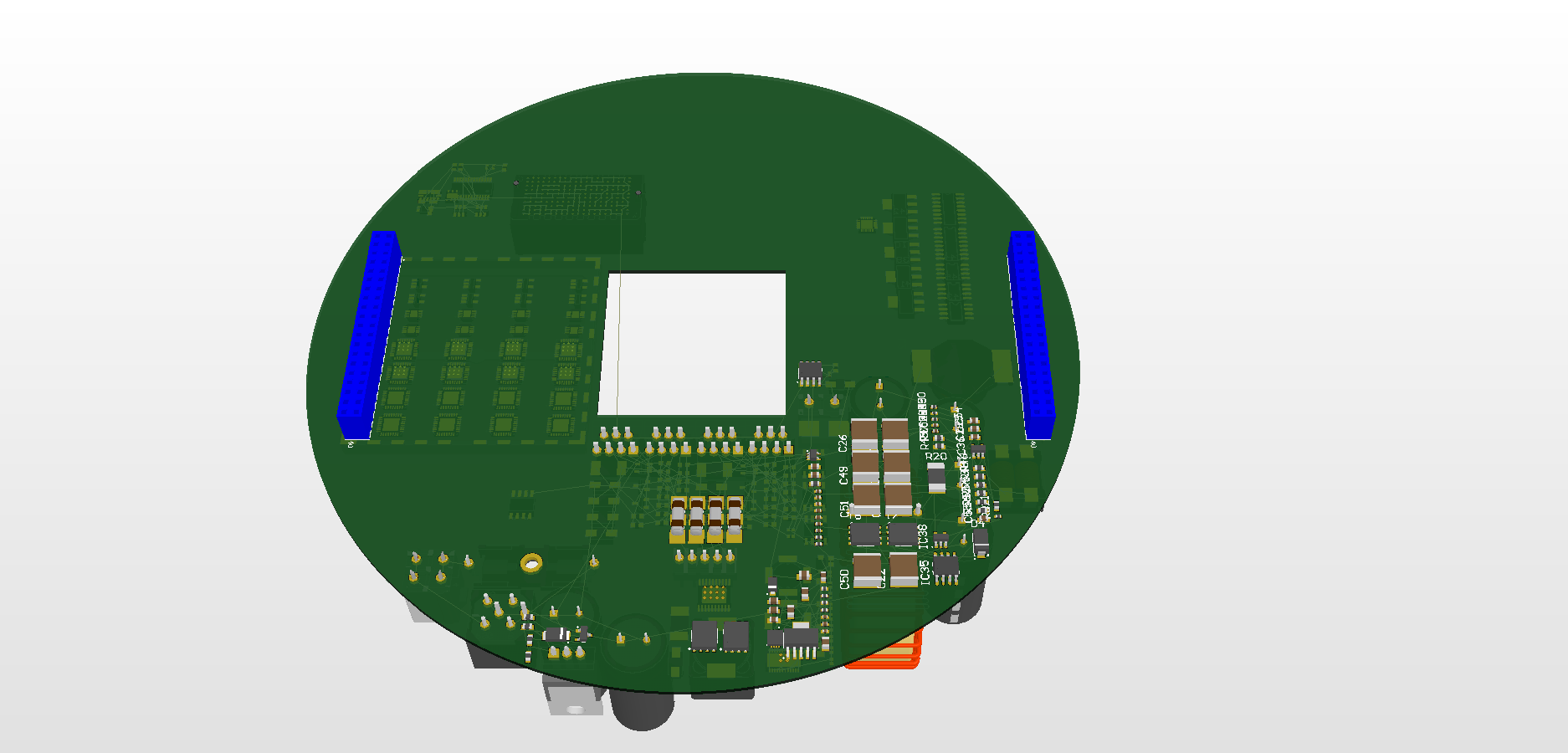
Objective lens will be heated with MOSFET current driver.

Shutter driver is implemented as a linear amplifier with current limiter (through feedback), working in half bridge configuration. Position detection will be based on electric capacity effect.

The Board also contains Peltier Thermoelectric Cooler (TEC) with a half bridge driver set trough a WM controller. An additional feedback circuit will be mounted on the Board to measure the Peltier module current. The PWM operation is synchronized with the CCD operation to prevent noise interference propagation to the AFE chain.

The Board also has a dedicated ADC used to read PT1000 temperature sensors measuring temperature in different parts of the camera. An additional integrated 3-axis accelerometer and temperature sensor will be placed on PCB.

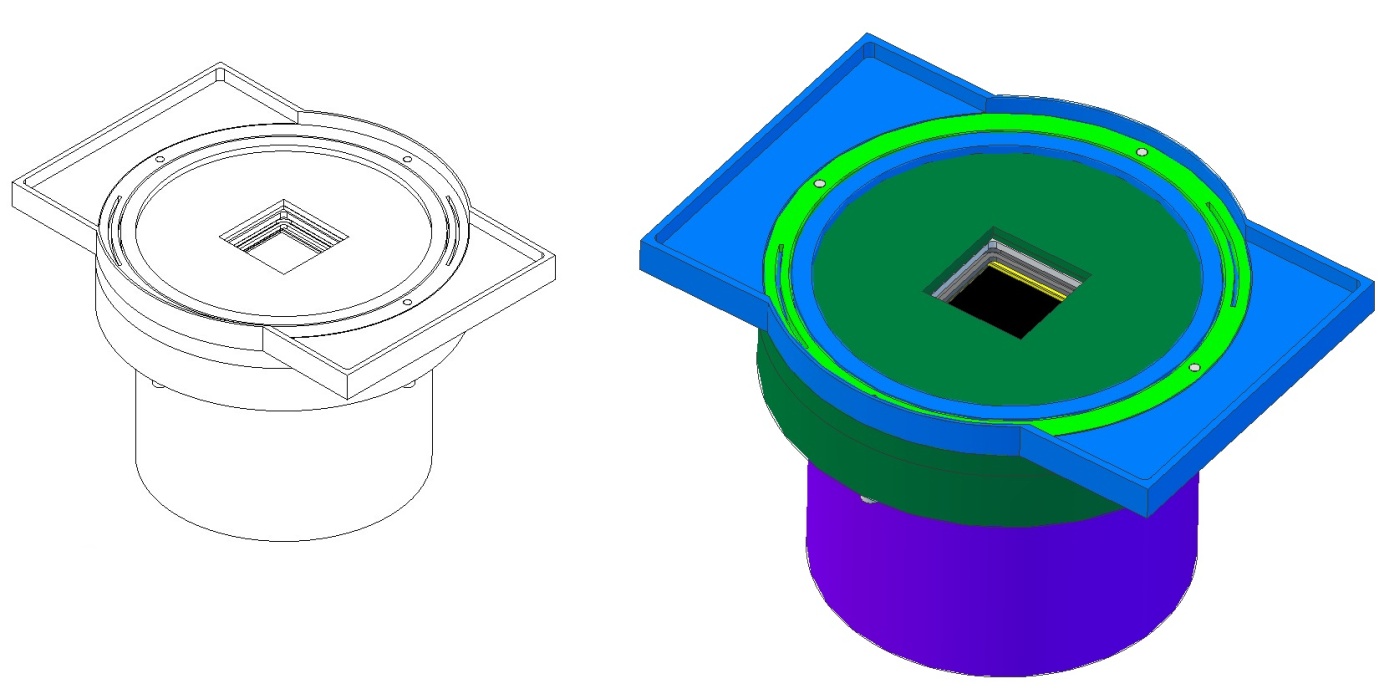


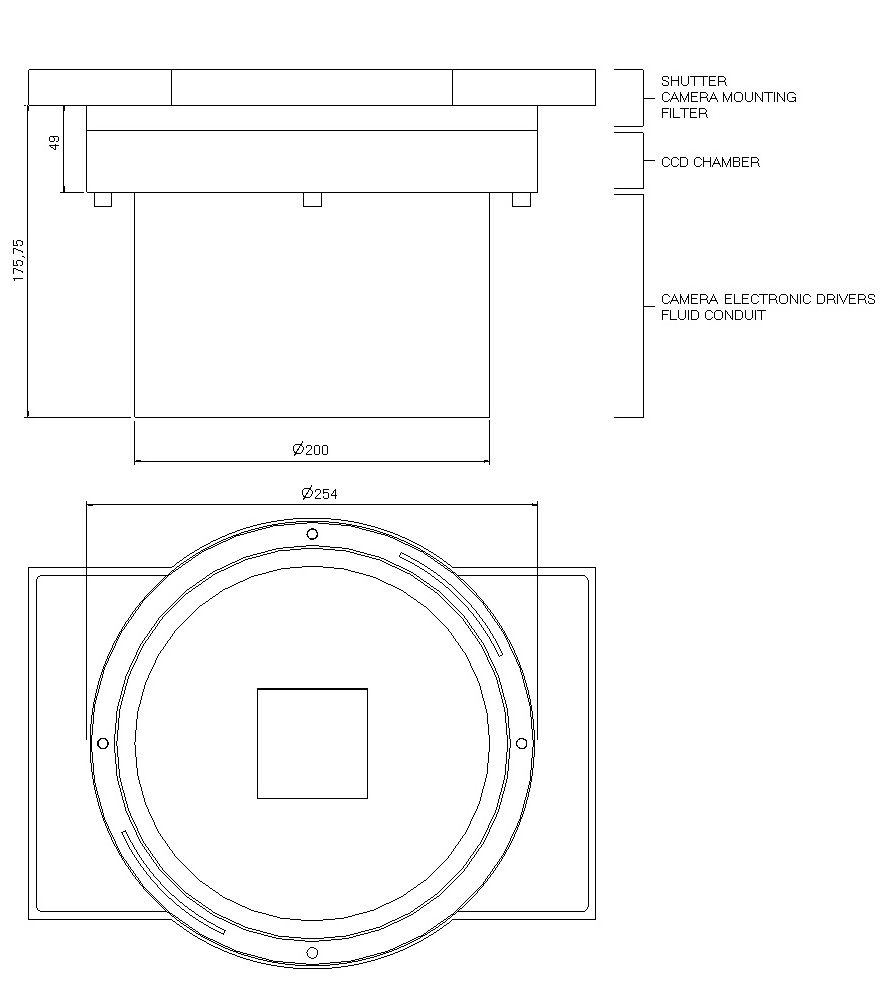


# Hardware – mechanics

## enclosure

Main materials the enclosure will be made of are aluminum and sheet metal. This way light weight design, reasonably low cost and high accuracy will be achieved.

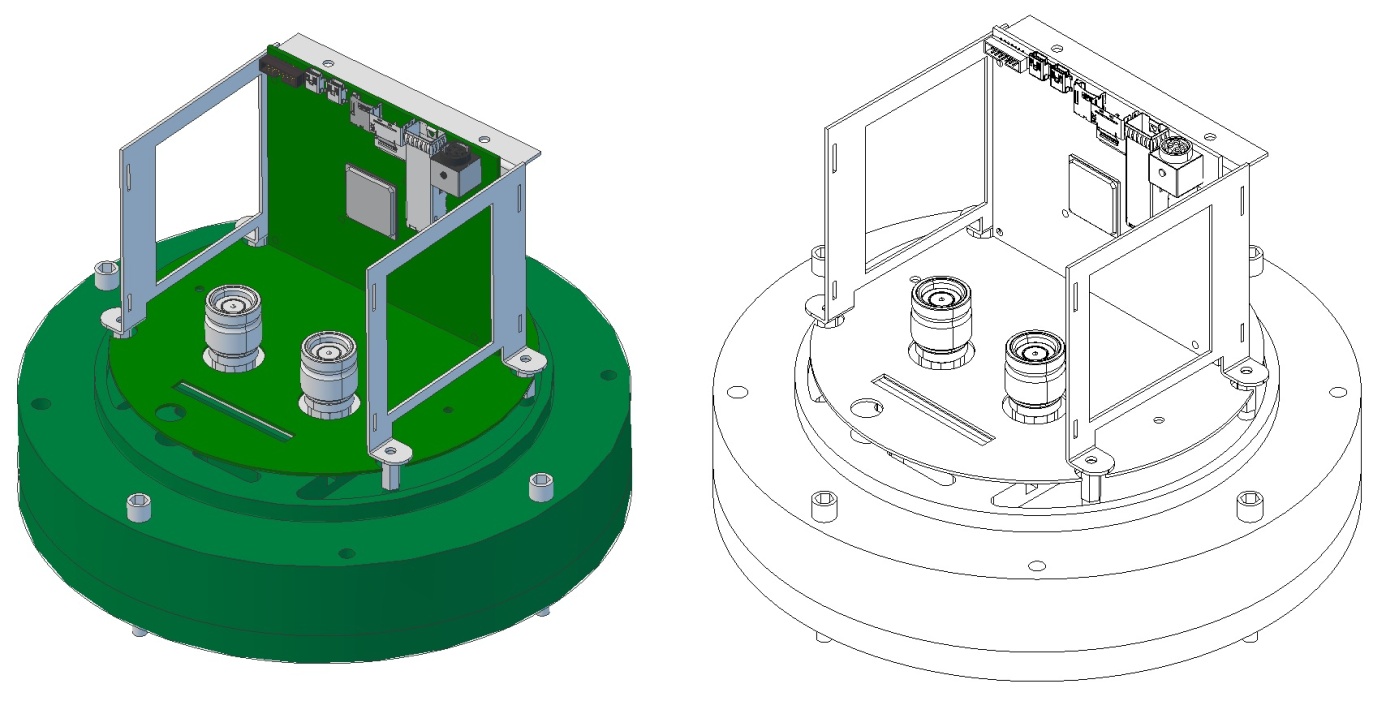




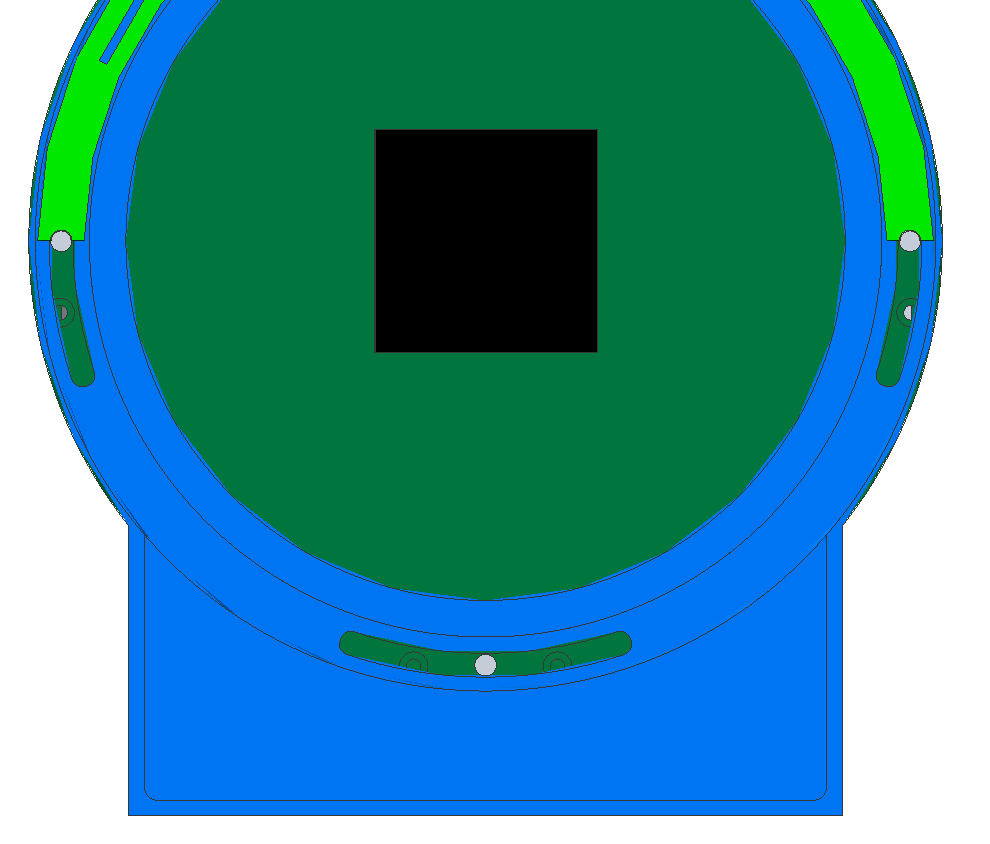
At the bottom part of the camera the following parts are installed:

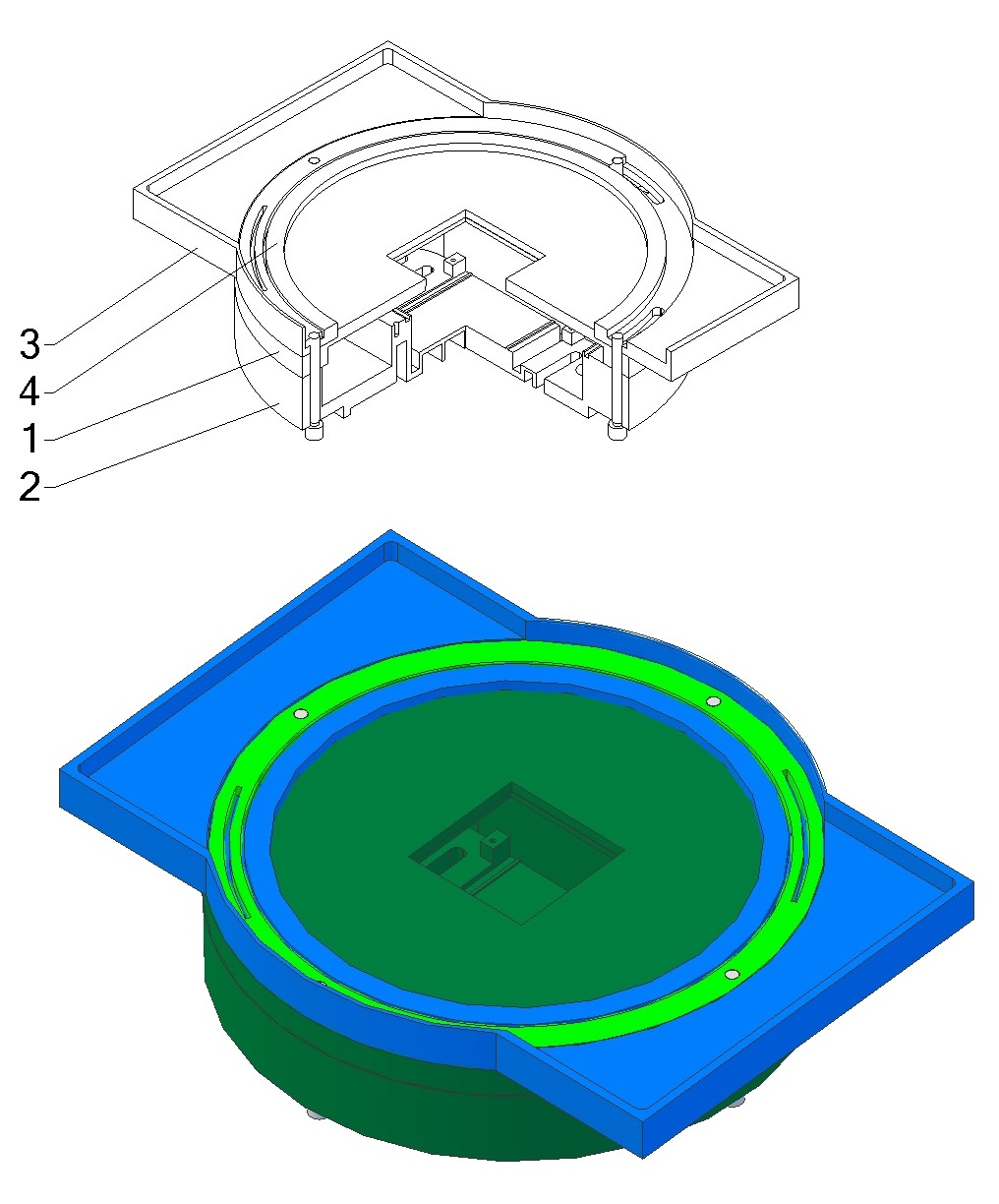
* CCD drivers
* TEC drivers
* shutter power stage and position sensor readout
* DC/DC power supply
* CCD Analog Front End and ADC module

The cover of that part of the camera is made of a round aluminum profile with a diameter of 200 mm. Electronic drivers are attached to the sheet metal frame that provides stability and positioning accuracy.



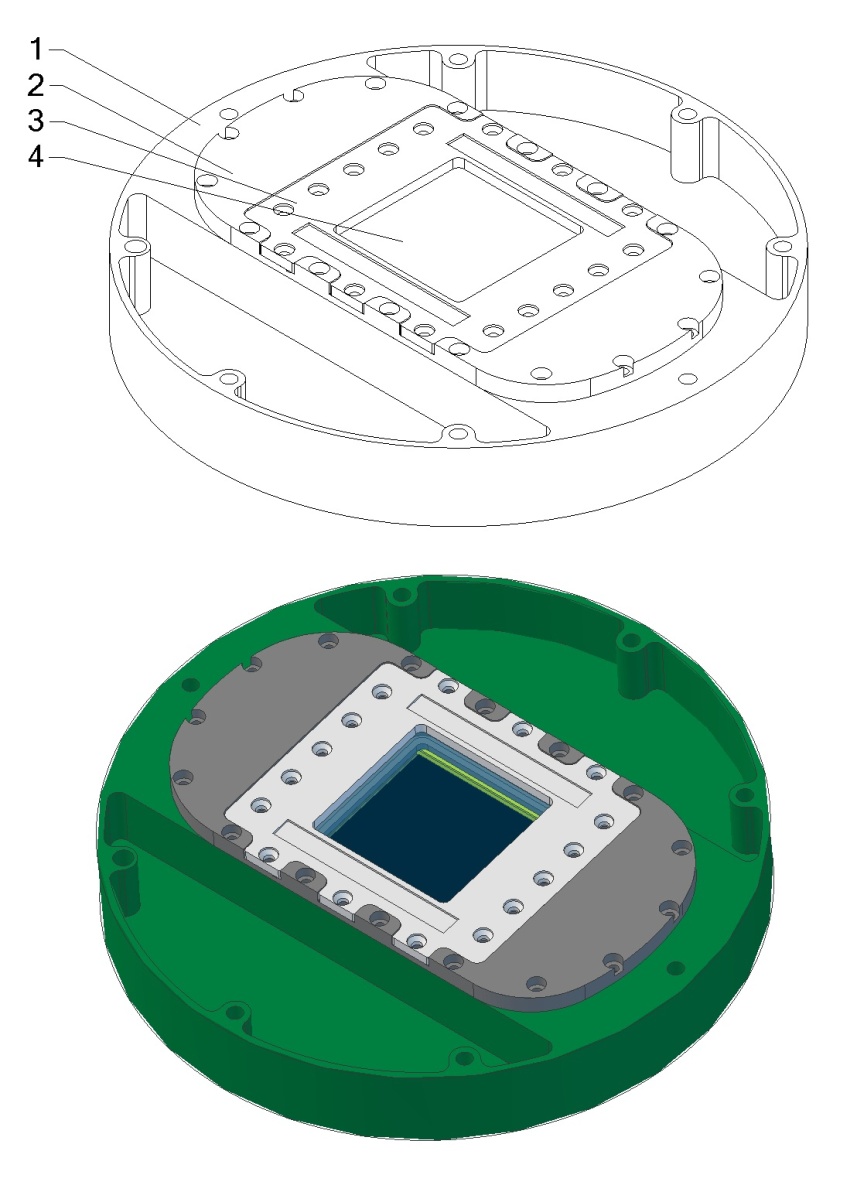
The issue of mounting the camera to the secondary mirror structure is still not determined because of the difficulty with fitting shutter into the original dimensions and because of appearance of new requirement to add a removable filter. One of the proposed variants is shown on the drawings below.

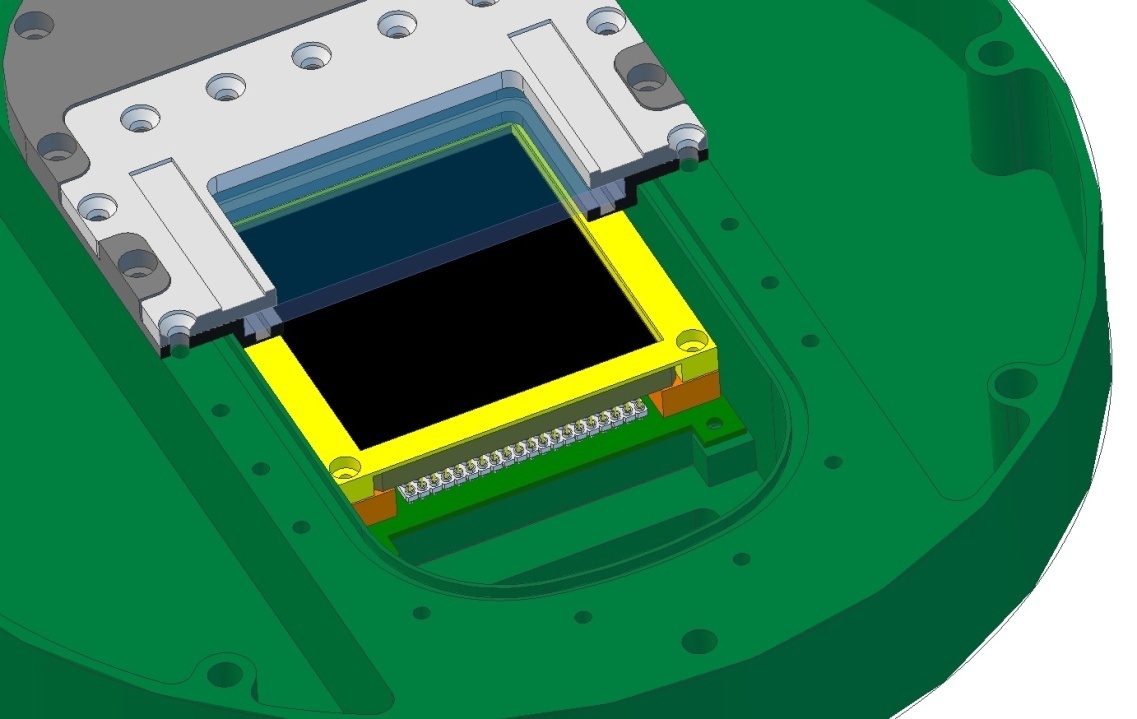




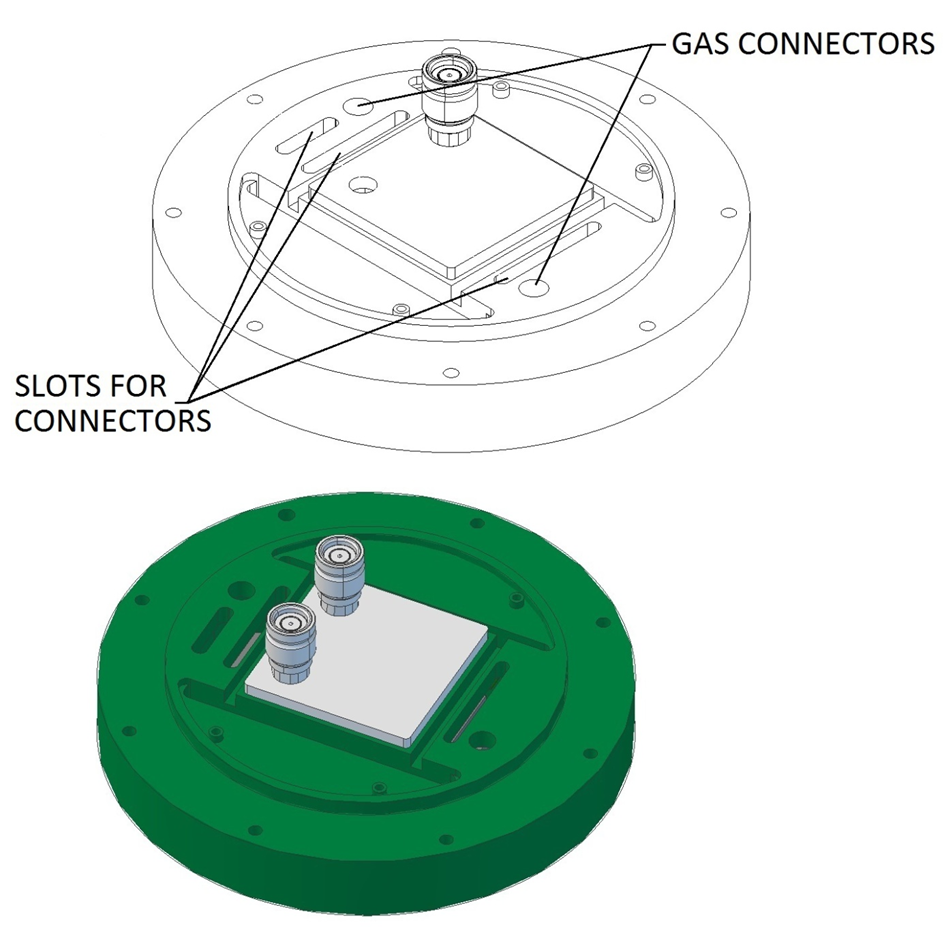
The screws pass the holes in the element 1 and 2, then pass through slots in the part 3 and then they are screwed into threads in a circular sheet metal 4. Slots in the element 3 allow for adjustment of the camera position during its assembly - rotation of 40 degrees. When the camera is adjusted the screws are tightened, what blocks the camera movement. The element 3 contains a removable filter and is attached to the secondary mirror structure, fastening details have not yet been established.

Construction of a sealed CCD sensor chamber is shown below.





The base element (1) is fixed to the top cover (2) and the glass suppressor (3) which provide the seal and sapphire glass fastening (4). Between the glass (4) and the cover (2) and between the base (1) and the cover (2) there are O-rings to seal the chamber. Between the cover element (2) and the glass suppressor (3), there is a heating element for heating the sapphire glass (4) in order to avoid the problem of condensation.



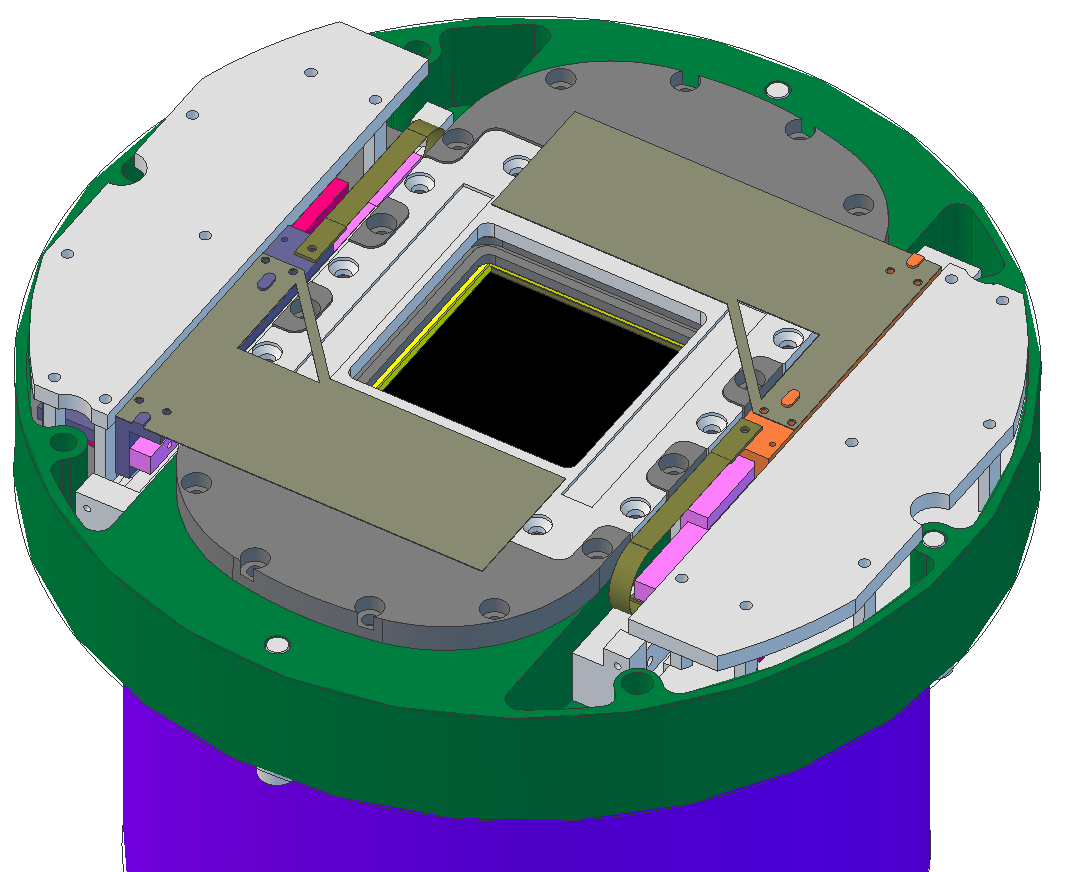
From the other side of the base element (1) there are holes for the gas connectors to fill the chamber with argon and the slots for 2.54mm pitch connectors (electronic signals and power). Connector slots will be filled with epoxy resin to keep the chamber sealed.

The external mechanical adjustment is in the process of design, it allows to set the sensor ± 1 mm from the nominal position.

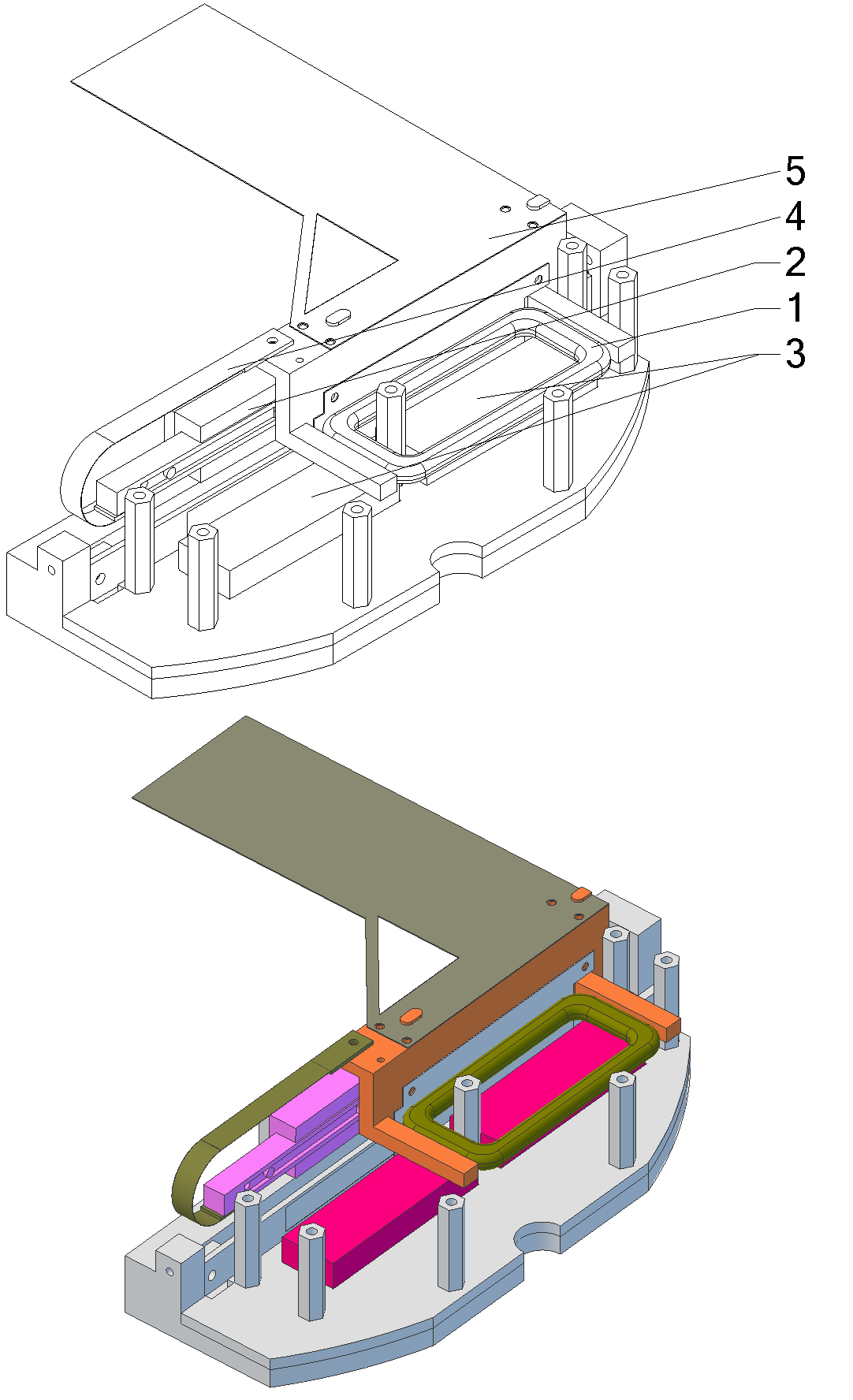
Inside the chamber there are pressure and temperature sensors to control the CCD temperature and to monitor seal of the chamber.

## Shutter

The shutter is installed in front of the sensor chamber in such a way that the heat generated by it does not interfere with the cooling of the sensor. There are two possible locations of the shutter: just above the sensor chamber or inside of the filter chamber, this matter has yet to be determined after the final settlement of the issue of mounting the camera.



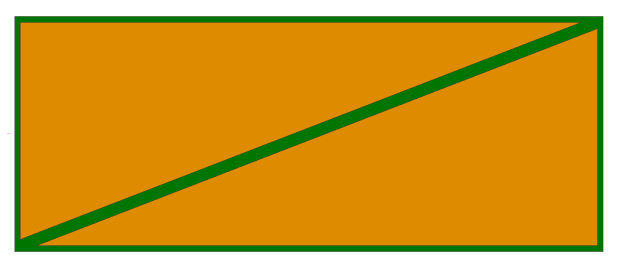
The shutter contains two identical modules based on a voice coil actuator. It consists of blades (5) four magnets (3), the coil (1), linear ball slides (2), holding elements and closing of the magnetic circuit. Shutter control signals are transmitted through the flex PCB (4).



The shutter performs linear motion under the influence of the Lorentz force which arises when current flows through the coil. This type of actuator is characterized by high dynamics and smoothness of movement. Neodymium magnets with high remanence are used to get the required power at low currents. Linear ball slides are characterized by small friction and high durability.



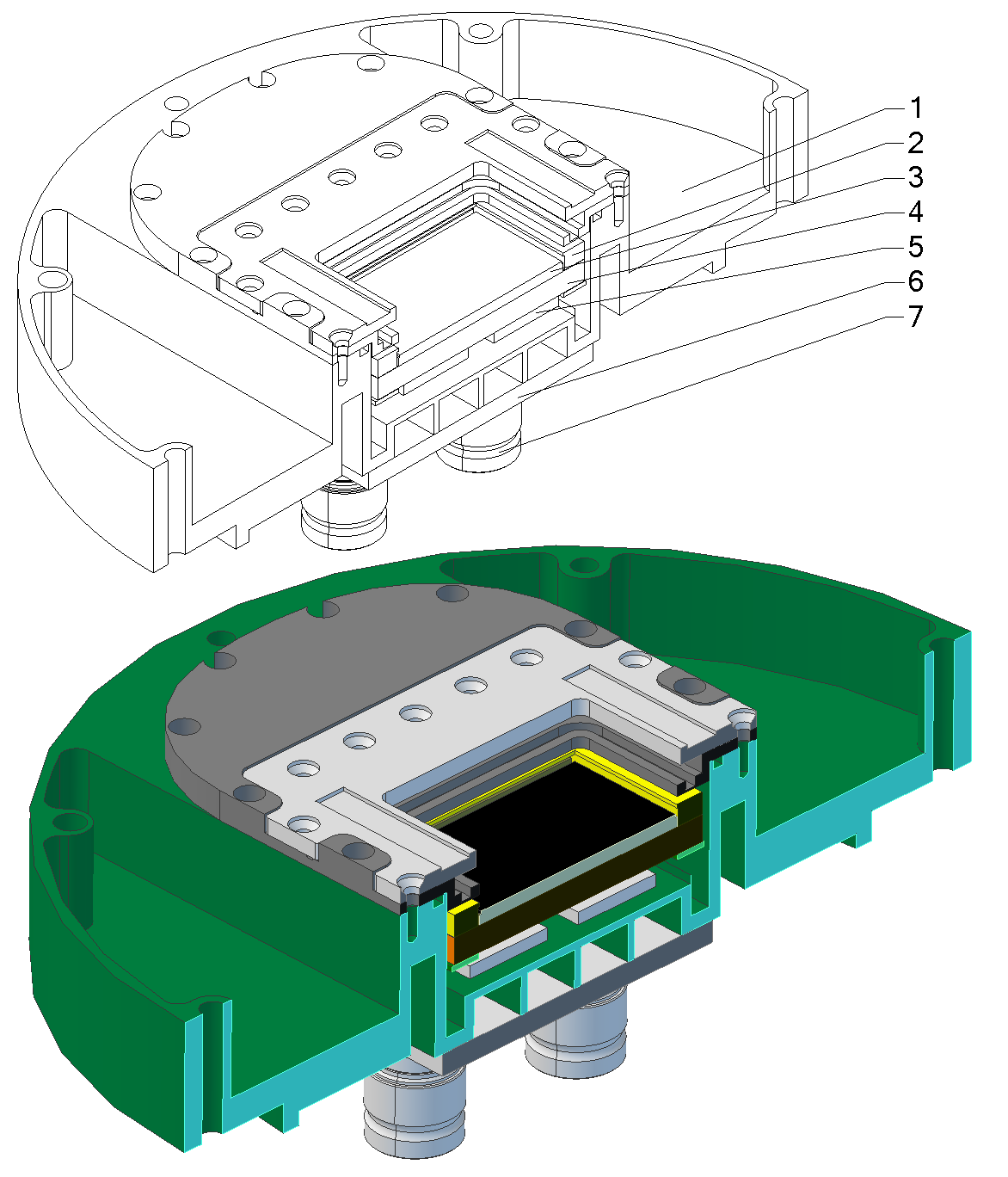
As a position sensor for shutter blades, a differential capacitive sensor is used. The principle of its operation is based on measuring the change in capacitance which is formed between the shutter blade and fields of copper on PCB underneath the shutter. PCB is placed in such a way that it is being covered and uncovered by shutter blades while it is moving.

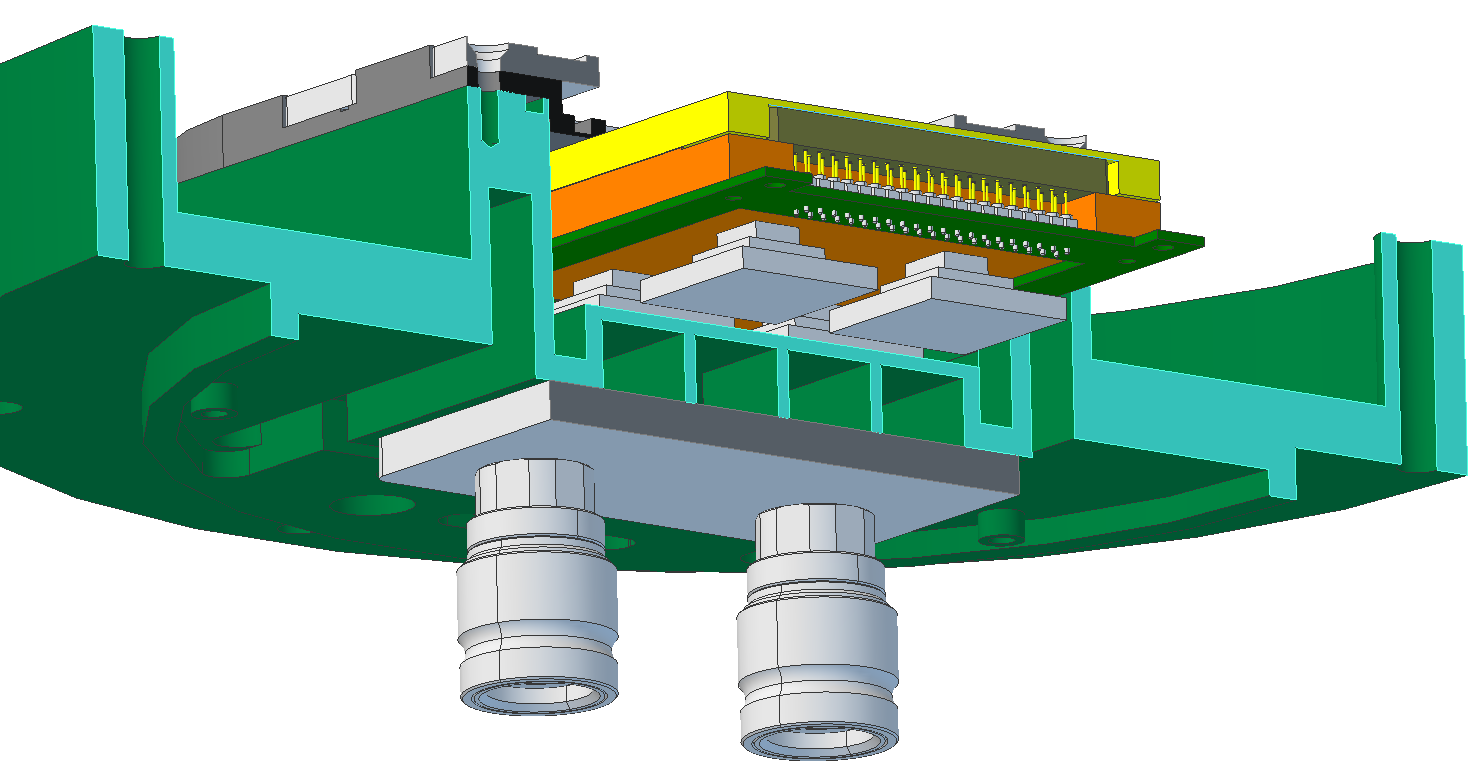


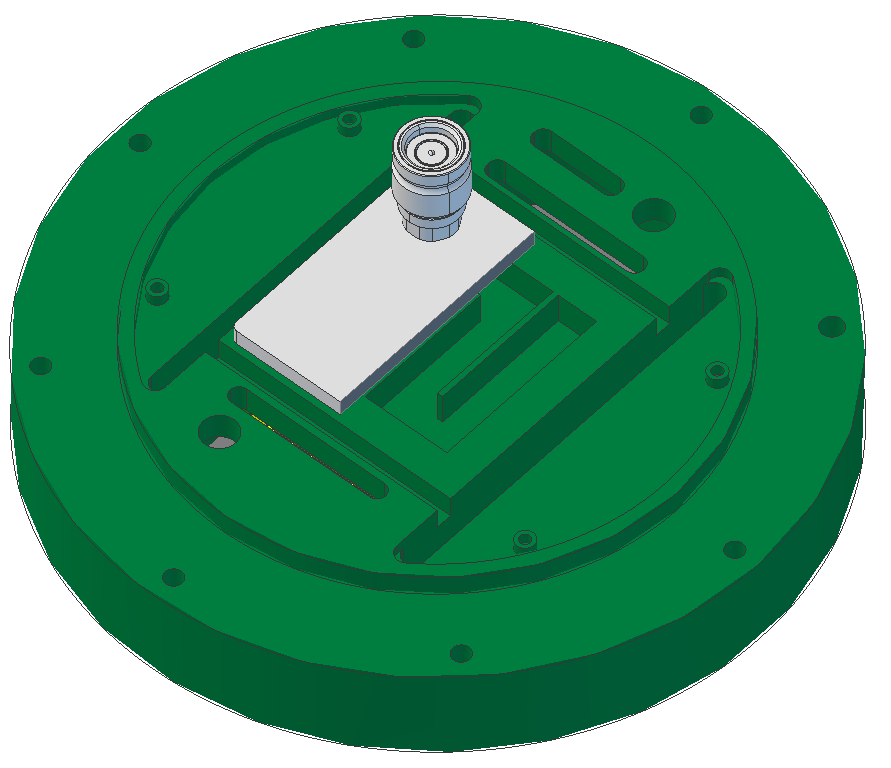
The PCB has two triangular fields which form plates of two capacitors, the shutter blades are the second plate for two capacitors. The triangulars are facing in different directions, so while a blade is moving, one of the capacitance decreases and the other increases so that a differential measurement can be used. Differential measurement eliminates the inaccuracies associated with the movement of the blades and the position of the PCB. To localize the blade, the sensor has to be calibrated first to know the relationship between output signal and the position of blade.

## Cooling system

The CCD sensor must be cooled to -50⁰C to ensure the low noise requirement. To do this, the sensor is cooled using four, three-stage Peltier modules from which heat is taken by a cooling block with the liquid (liquid cold plate). The cooling liquid is glycol and water. Below are drawings showing the thermal path in sensor cooling system.







The CCD sensor (4) is pressed by tightening element (2), made of a laminate, to improve the adhesion of the sensor surface to the copper block (4). The purpose of copper block is to spread the heat transferred to the Peltier module (5) from the entire surface of the CCD sensor. This eliminates temperature gradients on the CCD area.

The cooling block is a part of the base element (1), its cover (6) is welded to the base (1) which guarantes seal of the block. The cover has the connectors (7) to supply and receive the cooling liquid.

# Software and digital system

## Introduction

This part of the report presents the software and digital system design of NEOSTEL CCD Camera System specification. A description of the camera system is presented in Section 2, as well as the current state of the project. Section 3 contains a detailed system behaviour specification in regards to the operating system.

## General Specification

A figure in section 2 provides a general overview of the camera system. The Mainboard with a CCD sensor and peripherials is connected to the Communication Board which controls the whole system.

## Description

The system described in this document should be treated as a standalone control and measurement system in form of an intelligent camera with broad spectrum of instruments to interface at the facility level.

The hardware is based on Xilinx Zynq SoC, which incorporates two core Cortex A9 application processors and an FPGA in one package. It also contains a number of integrated peripherals like Ethernet, SPI, I2C, CAN, USB etc. and an DDR3 memory controller.

The system runs both Linux and RTOS operating systems in an AMP scenario. Linux is responsible for high level control and maintenance and RTOS for time critical tasks.

Communication is based on Ethernet. It provides microsecond synchronisation capability due to the use of the PTP synchronisation protocol. RS485 also is used in the system as a standard console output.

An interface for CCD sensor analogue front-end and a shutter mechanism are implemented entirely in logic in order to provide exact timing control.

The system is controlled via EPICS with implemented server functionality. The picture data will be double buffered and sent in FITS format to remote facility server.

## System Features

* Low noise 16MP CCD sensor readout – pictures are in self describing FITS format with additional diagnostic information
* Shutter control with accurate start/stop position feedback implemented in FPGA
* Environment measurements (humidity, temperature, position)
* EPICS SCADA support with EPICS server implementation for system diagnostics and control
* High speed interface: 1 Gbps Full Duplex Ethernet through SFP transceivers with full hardware PTP support including hardware time stamping
* Internal and external trigger
* Time synchronisation via PTP
* Heterogeneous system with both RTOS for critical procedures and Linux for interfacing flexibility and easy data processing with low latency control and diagnostics path
* Universal CCD data readout with flexible FPGA logic and modular AFE
* Innovative Xilinx Zynq design with dual core Cortex A9+ and FPGA on one die with shared subsystems

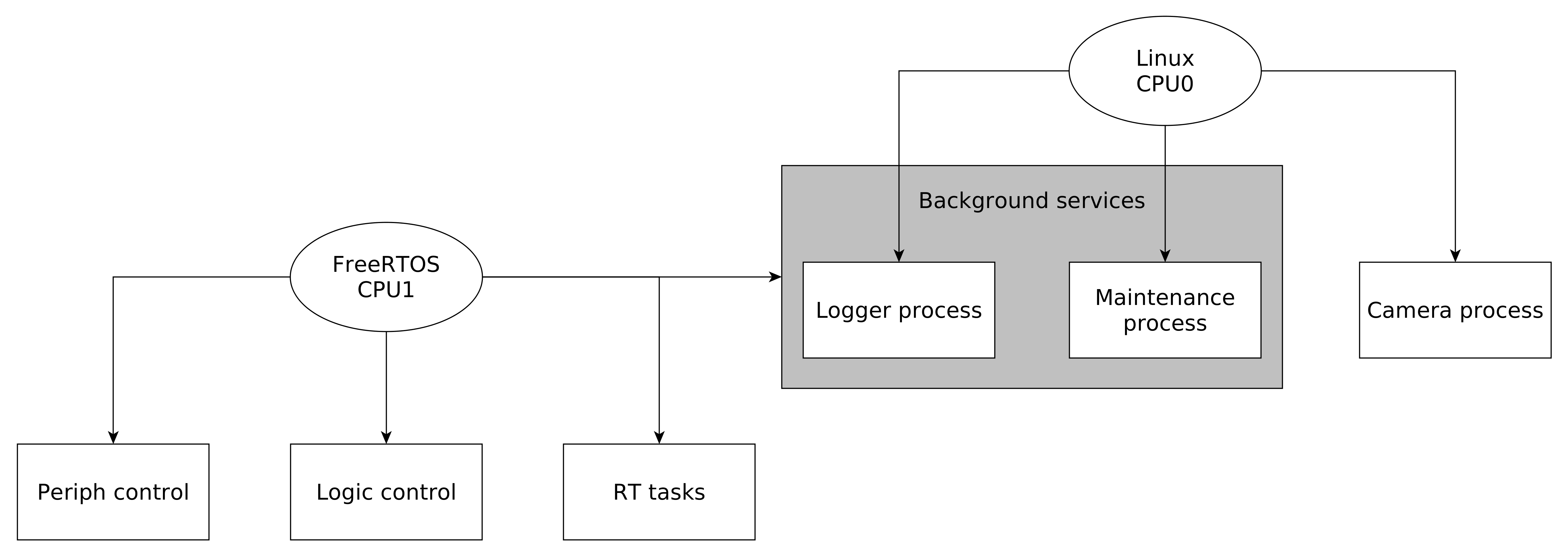
## Specification

This part of section describes the specification of the NEOSTEL camera system with detailed diagrams of system behaviour.

### Operating system

#### Architecture

The Camera operating system architecture is shown on the diagram below.



The Camera is running two operating systems. An embedded Linux system and RTOS. Linux is used for communication and control of the whole system and RTOS is used for time critical tasks.

SoC that is used in this design is a two core unit which supports the AMP operation. This way one core is used for Linux and the other is for RTOS.

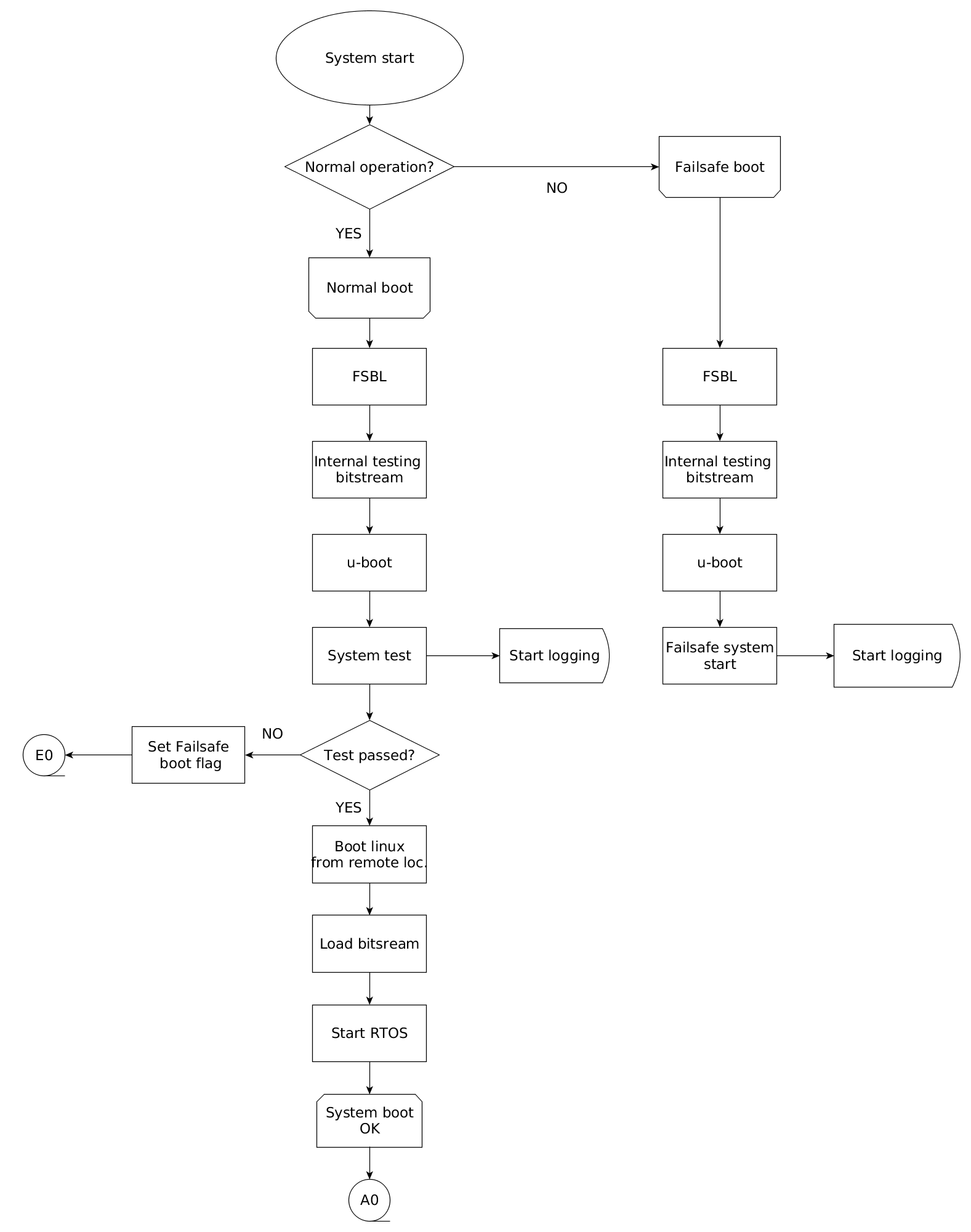
#### Boot sequence

When input power is applied to the camera, the system starts booting. Initial boot sequence works as pictured on the diagram.

Boot sequence incorporates initial system test. Basic peripherials needed for operation are checked. Because of the fact that the system is a multi-camera design, the operational system image is stored remotely. (e.g. on a server available via NFS).

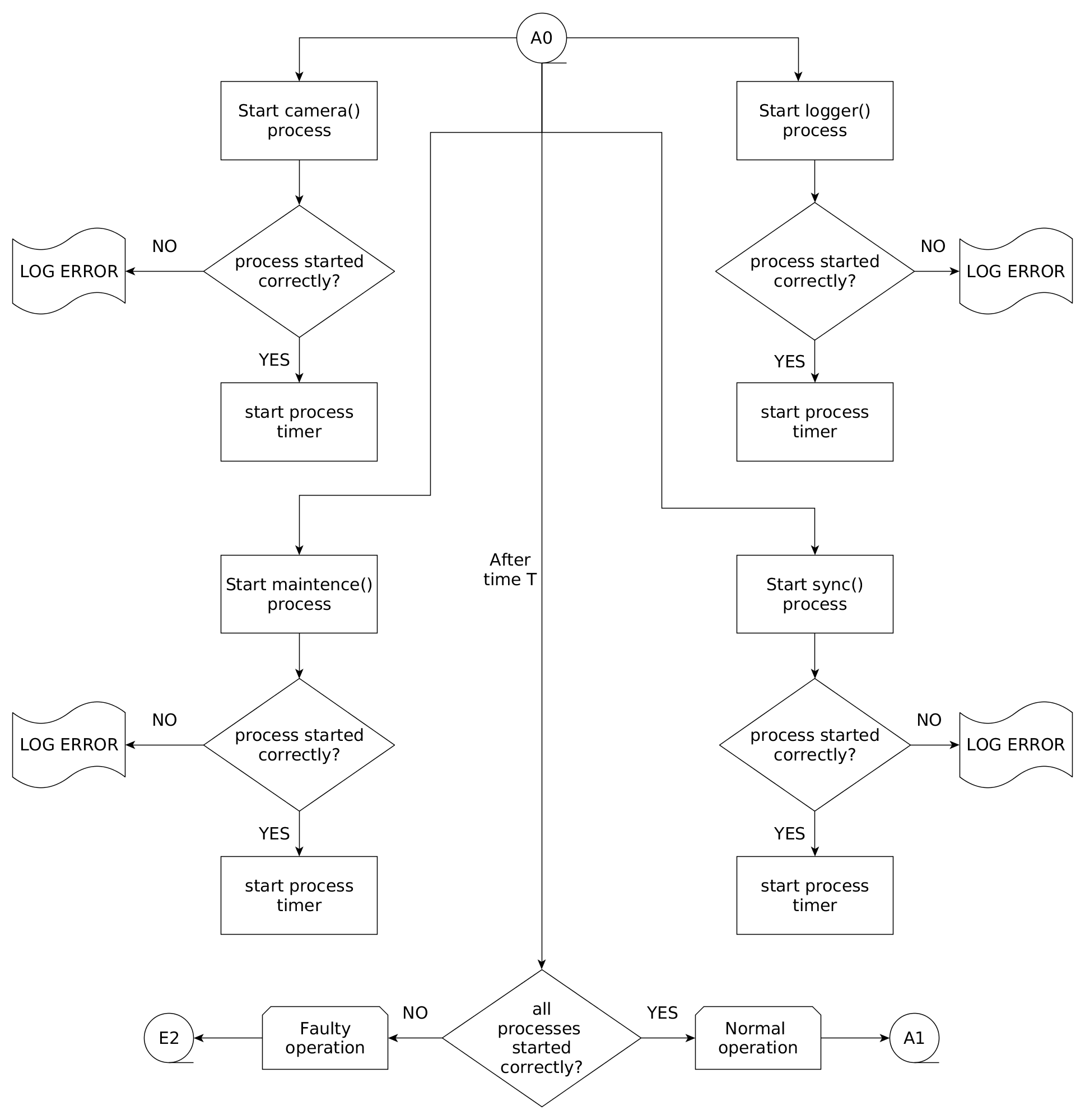
Initially a testing version is booted from QSPI Flash memory, if the initial test has passed, the remotely available image is loaded and the system is restarted. In the second scenario a fail-safe system version is booted.

Initial testing will be done using uboot procedures. All of the diagnostic output during the boot is logged on a SD card attached to the designed board to enable future problem tracing and debug possibilities.



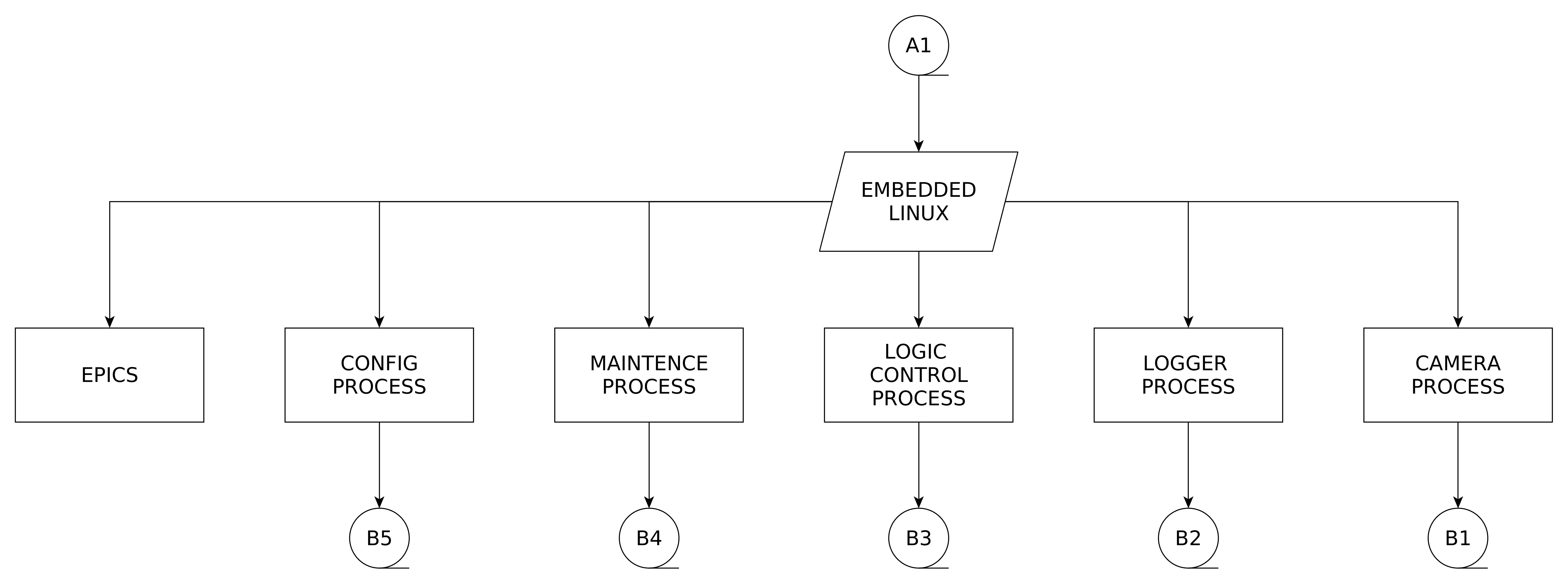
### Linux start

The Linux start sequence is shown below.



After a correct boot procedure Linux OS starts all processes needed for proper operation. These processes are responsible for controlling all peripherials and CCD data acquisition. At this moment normal embedded Linux OS is running and all typical applications and access methods such as ssh are available. Logs are stored internally on a SD Card and additionally they can be send via EPICS to the control system or viewed through a serial console. If all processes started correctly the system is moving to the A1 state, which is a normal operation. In the second scenario the system goes to E2 state which means that some subsystems are not fully operational.

### Operating system normal operation



The scheme above shows the normal system operation. Embedded Linux is running along with all processes. EPICS control is using processes and programs that control all of the peripherials.

At this point the system can be controlled via EPICS or manually by logging directly to the system.

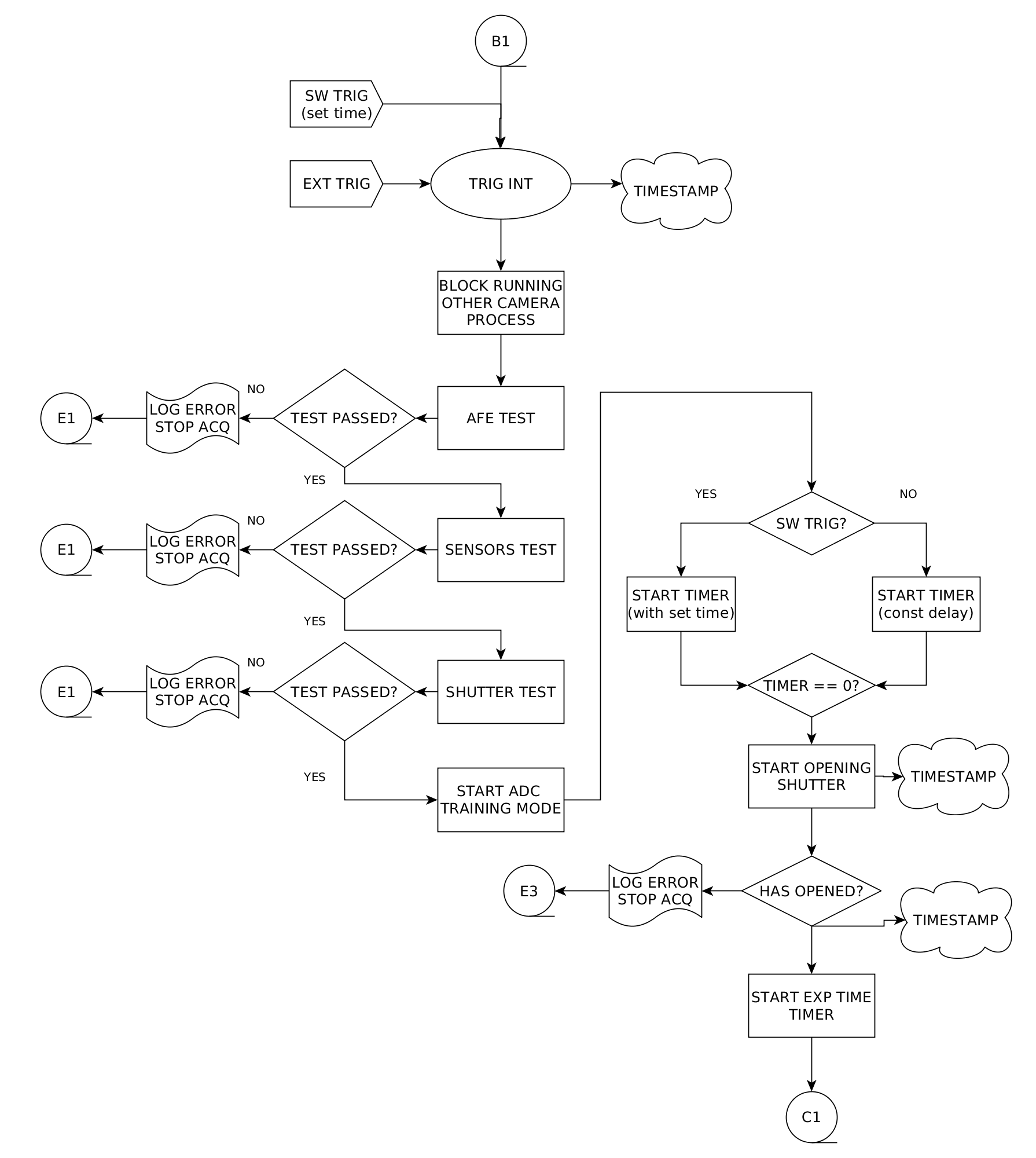
The initial setup script that is being run at the beginning of the boot sequence provides default configuration of the device.

The processes that are running on the camera are responsible for:

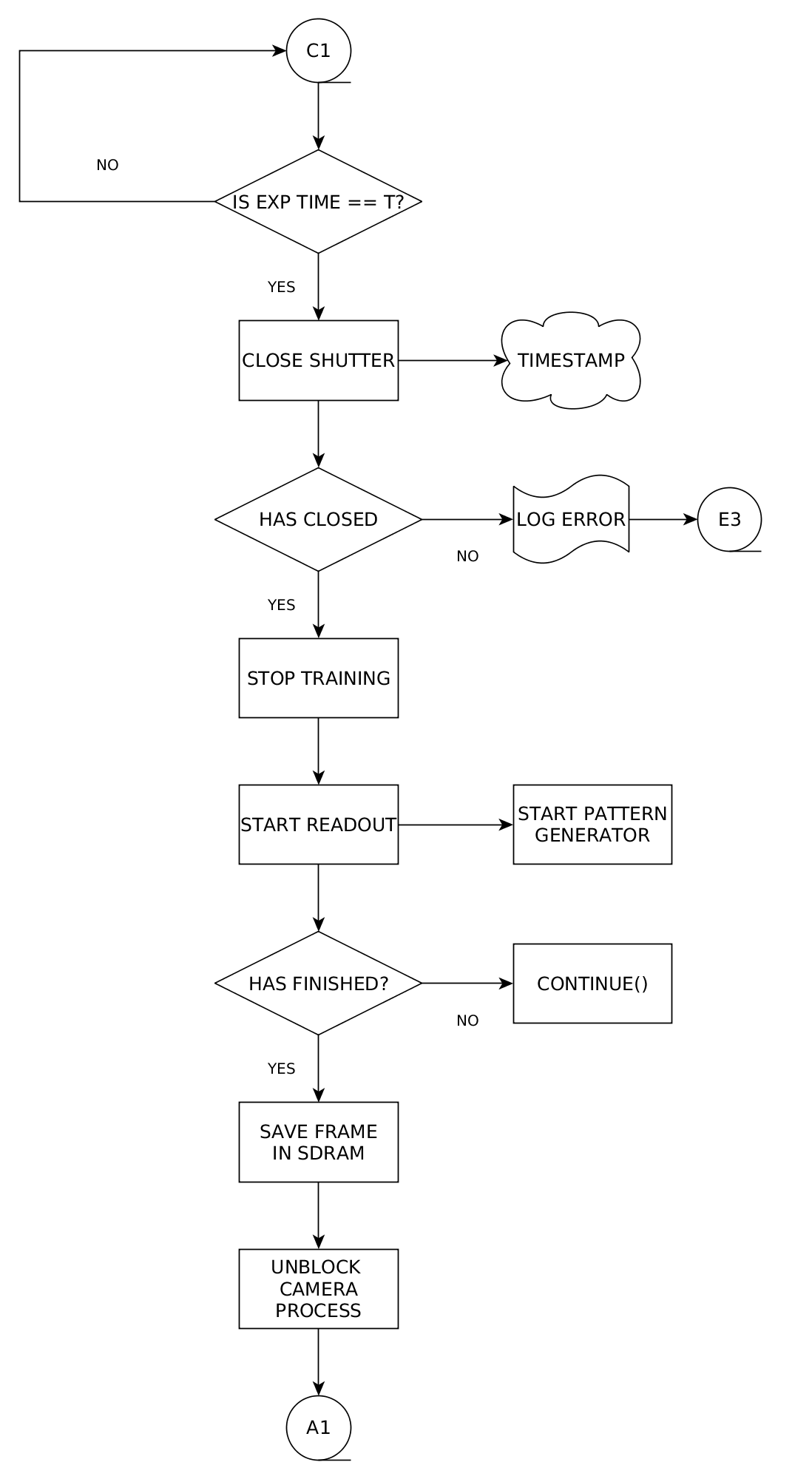
* maintenance – checking all peripherals and runtime behaviour
* configuration – for set-up of camera configuration
* logic control – IP Cores control and set-up
* logging – storing all system behaviour
* camera control – pictures acquisition, shutter and readout control.

### Camera process

The scheme below shows the system behaviour when the image trigger is started. First basic testing is run to check if all systems are operational. Then shutter opening is started.



Camera process behaviour after opening the shutter is shown below. A Shutter opening and CCD readout are timestamped. Along with time, the sensor data are stored for each timestamp. Timestamping itself is done in the processing system. The precision of this approach is equal to approx. 3 µs. After the shutter opening exposure time is measured and when it's finished the shutter closure procedure is started. Both opening and closing of the shutter can fail, in this scenario the camera process is terminated and disabled.



Operation of other processes running in the background are shown below.

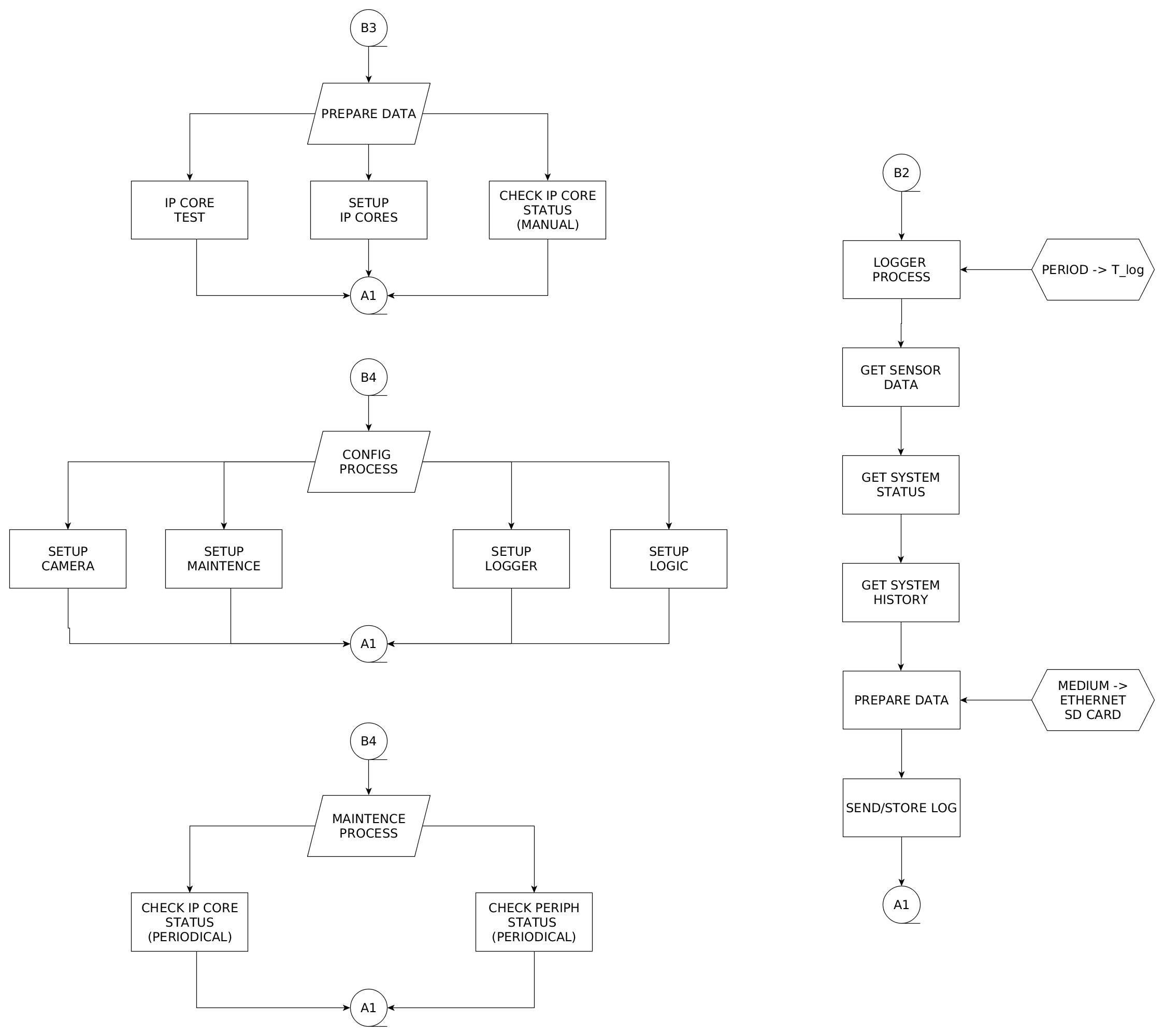
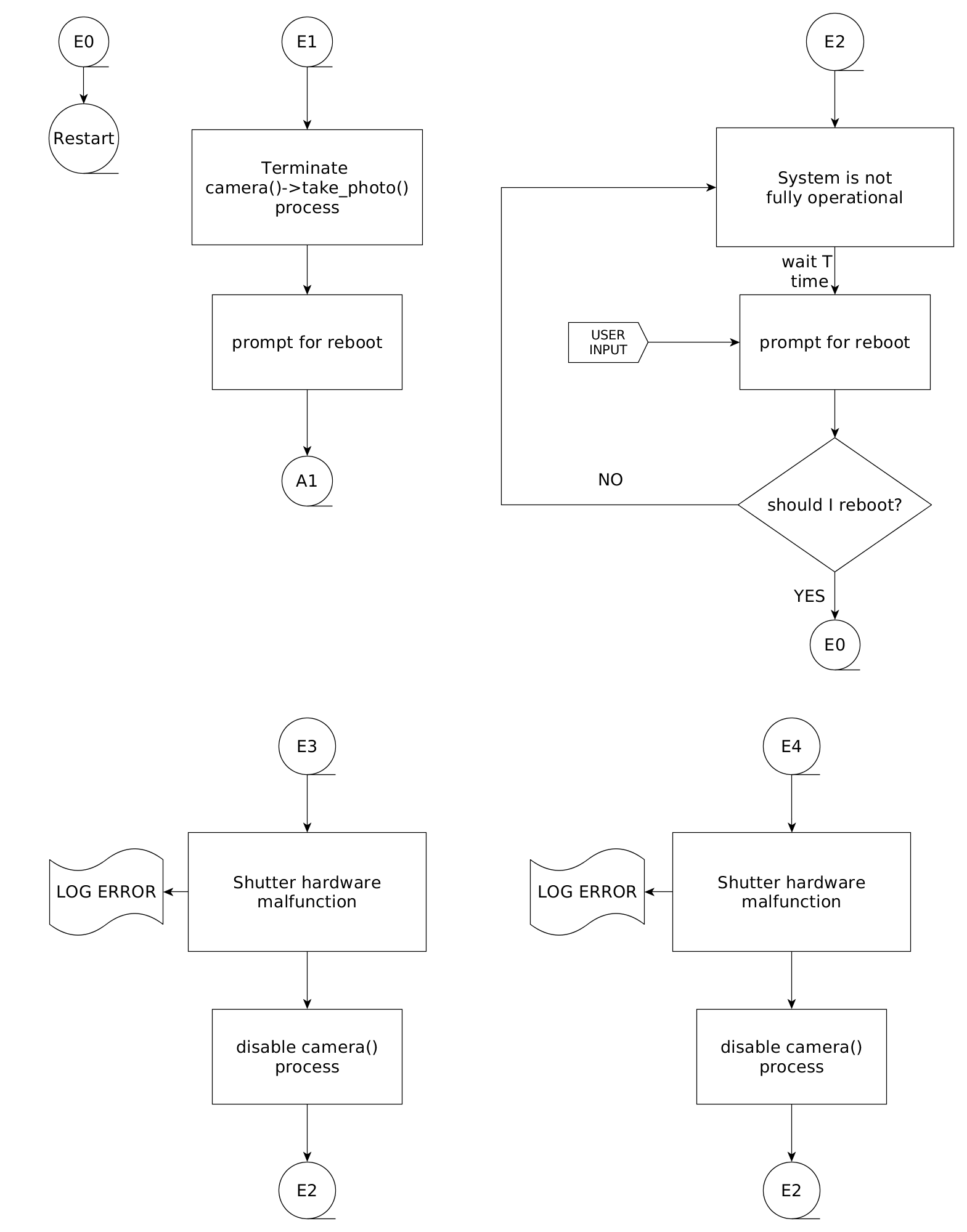


Diagram below presents errors handling processes.



### Acronyms

|  |  |
| --- | --- |
| **AD** | Applicable Document |
| **CGS** | Compagnia Generale per lo Spazio (formerly Carlo Gavazzi Space) |
| **NEOSTEL** | NEO Survey Telescope |
| **FPGA** | Field Programmable Gate Array |
| **SoC** | System on a Chip |
| **CCD** | Charged Coupled Device |
| **GbE** | Gigabit Ethernet |
| **PTP** | Precision Time Protocol IEEE1588 |
| **EPICS** | Experimental Physics and Industrial Control System |
| **FITS** | Flexible Image Transport System |
| **MP** | Mega Pixel |
| **AMP** | Asymmetric multiprocessing |
| **RTOS** | Real-time operating system |
| **SFP** | Small form-factor pluggable |
| **AFE** | Analog Front End |
| **IP core** | Intellectual property core |
| **SPI** | Serial Peripheral Interface |
| **I2C** | Inter-Integrated Circuit bus |
| **CAN** | Controller area network |
| **Uboot** | DENX Universal Bootloader |
| **USB** | Universal Serial Bus |
| **DDR3** | Double data rate RAM, third generation |
| **RAM** | Random access memory |
| **UART** | Universal asynchronous receiver/transmitter |
| **SD** | Secure Digital memory card standard |
| **QSPI** | Quad SPI |
| **NFS** | Network File System protocol |
| **SCADA** | Supervisory control and data acquisition |